**A TCAD Study on Simulation and Benchmarking of Nanometer Scale**

**Functionally Graded Materials as Gate Dielectrics for FinFETs**

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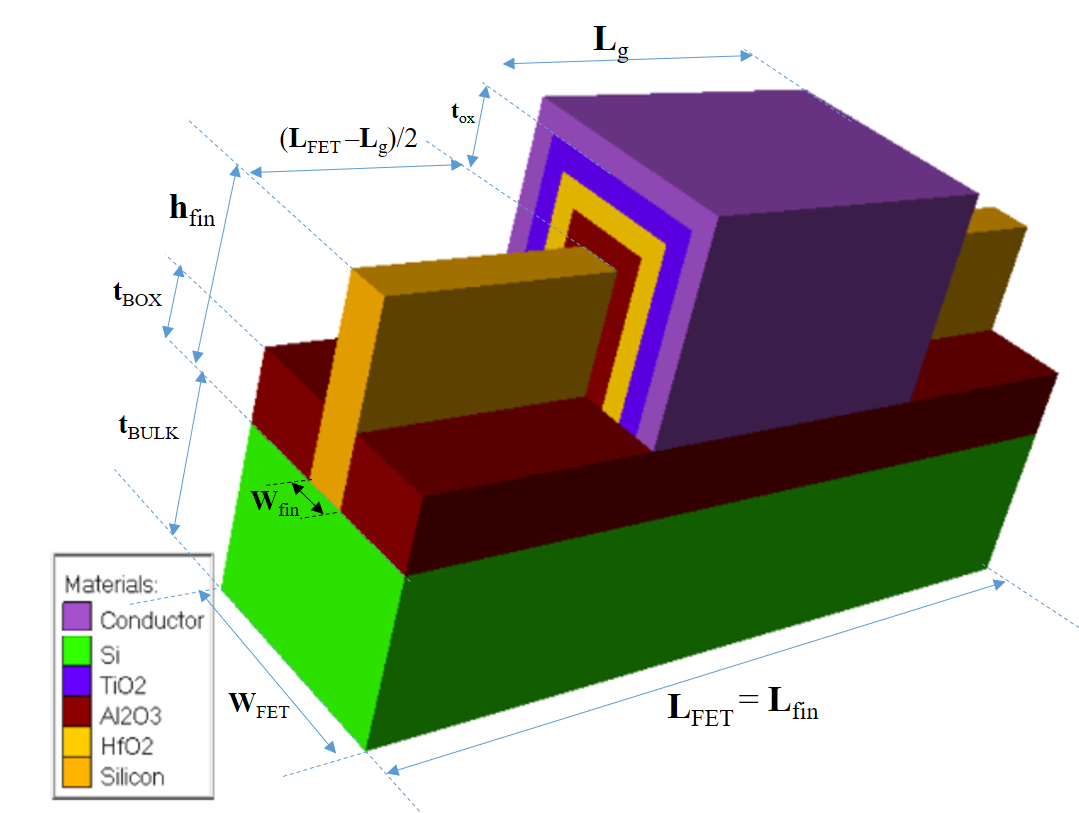
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**ABSTRACT**

In this paper, we present simulation results obtained using TCAD tools for a 3-D silicon on insulator (SOI) n-FinFET structure with various functionally graded materials (FGMs) as gate dielectric, with a gate length of 14 nm at 300K. Study explores the potential of FGMs as a viable alternative to conventional single layer high- dielectrics in FinFET structures. We investigate the impact of using FGMs as gate oxide dielectric on key electrical performance parameters, threshold voltage (**V**TH), on-state current (**I**ON), off-state current (**I**OFF), drain-induced barrier lowering (**DIBL**) and subthreshold slope (**SS**), **I**ON/IOFF ratio and gate metal-to-silicon leakage current (**IGL**). Using SILVACO ATLAS for device simulation, we start with SiO2, Al2O3, HfO2, La2O3 and TiO2 as single layer gate dielectrics of 3nm thickness (**t**ox) for a 14nm channel (fin) length (**L**FET), 2nm channel width (**W**FET), 5nm channel height (**h**fin) FinFET structure; then formed 13 different 2- or 3-stage FGM combinations as gate dielectrics, like [Al2O3:HfO2:TiO2] staged in parallel sheets, connected serially, as a 3-stage example. Modified Penn Model [1], [2] is used to calculate the dielectric constant of thin nanolaminate material forming each FGM laminate, using their bulk dielectric constant bandgap energy EG, high frequency dielectric constant and its Fermi wave vector *K*f. Maxwell-Garnet (MG) approximation [3] is selected to calculate the effective dielectric constant () for the 2-and 3-layered FGM dielectrics. Hot Electron / Hot Hole Injection (HEI-HHI) model [4] is used to model gate leakage current within SILVACO ATLAS/Deckbuild simulation tool and results were found to be consistent with experimental results within [5], with systematically varying thickness of mentioned dielectric layers to form a graded structured 3 nm-thickness FGM gate dielectrics. FinFET Buried Oxide (BOX) material was kept as Al2O3 through all simulations. Our results indicate that proposed FinFET with FGM gate dielectrics has lesser IGL up to 53 times, lesser DIBL up to %38.2, lesser SS up to %7.6, lower IOFF up to 2 decades, higher ION up to %62, higher ION/IOFF up to 45 times and lesser VTH up to %19.2, with respect to the FinFET of same dimensions composed of single layer HfO2 gate dielectric. FGMs show better performance than single material dielectric when used as gate insulating materials. Results may provide versatile opportunities for optimizing FinFET devices.

**Keywords**: Technology Computer-Aided-Design (TCAD) Simulation, Functionally Graded Material (FGM), Junctionless Thin Film Transistor (JLTFT); Fin-Field Effect Transistor (FinFET), Drain Induced Barrier Lowering (DIBL); Subthreshold Slope (SS), Threshold Voltage (VTH), ION/IOFF ratio.



Gate

Channel

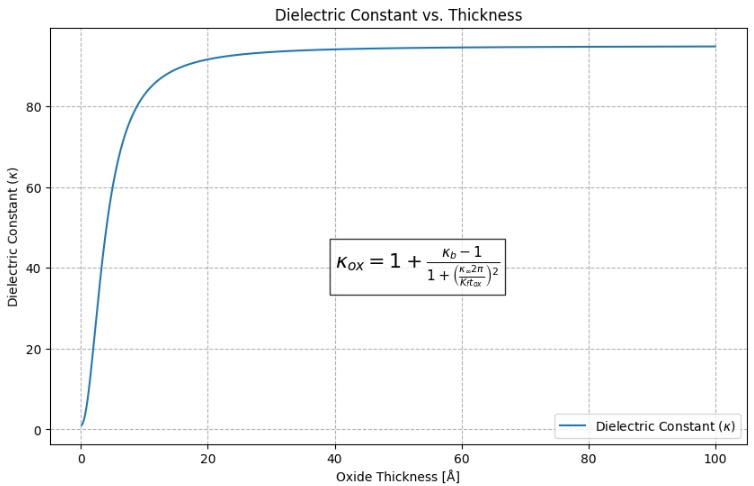
Buried Oxide (BOX) on Silicon

Figure 1. Proposed 3-material FGM gate oxide dielectric based FinFET Şekle BOX caption ekle

metin, diyagram, ekran görüntüsü, çizgi içeren bir resim

Açıklama otomatik olarak oluşturuldu

Figure 2. Stepwise Grading Profile for an example FGM (FGM-H in Table 4B.) as gate oxide dielectric

 metin, diyagram, çizgi, öykü gelişim çizgisi; kumpas; grafiğini çıkarma içeren bir resim

Açıklama otomatik olarak oluşturuldu

Figure 3. Modified Penn Model for dielectric constant against thickness applied to TiO2 [1], [2].

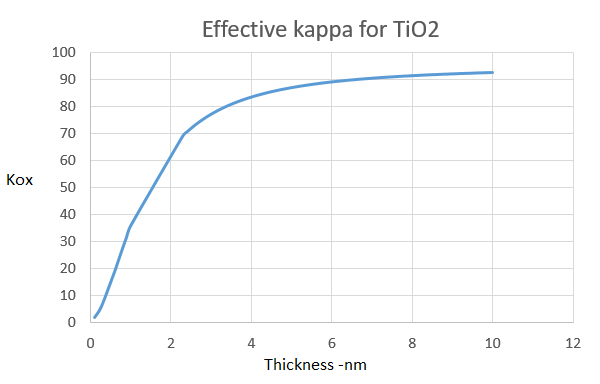


Figure 4. A numerical approximation for Penn Model evaluated by Equation-2

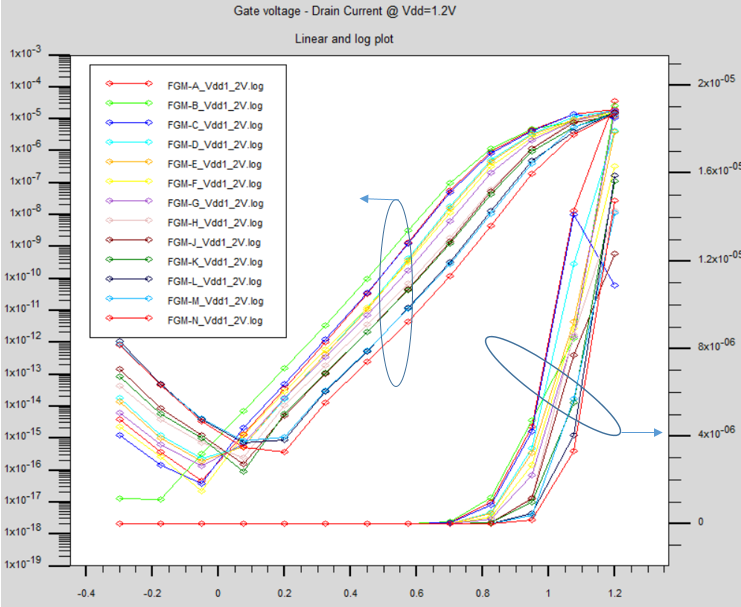
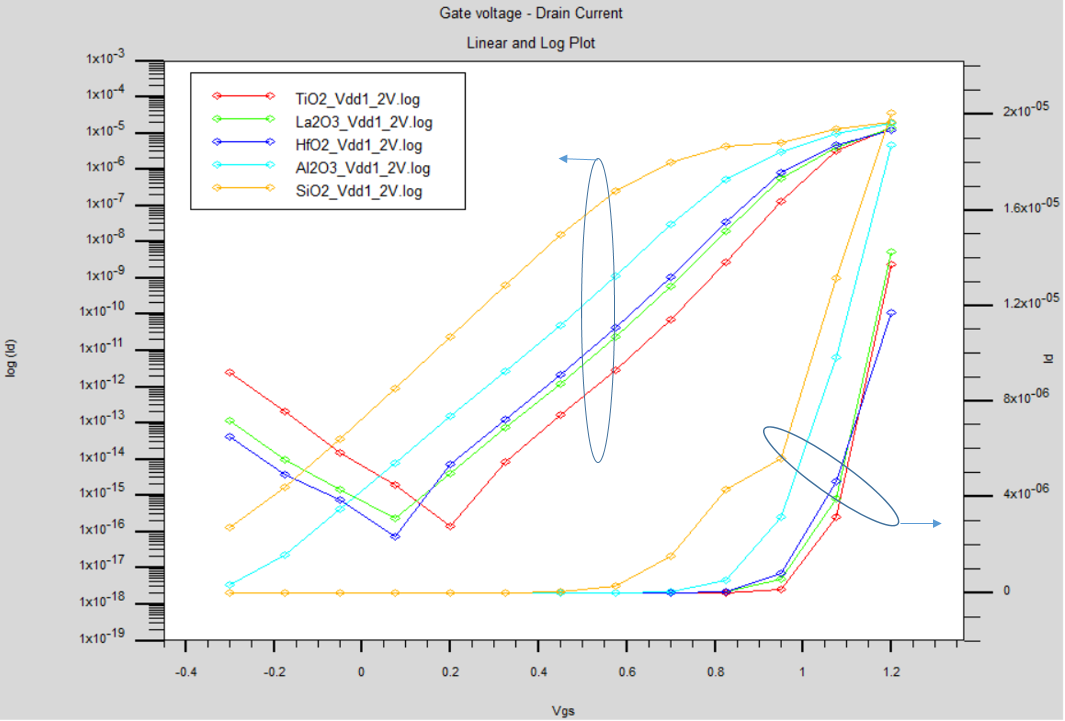
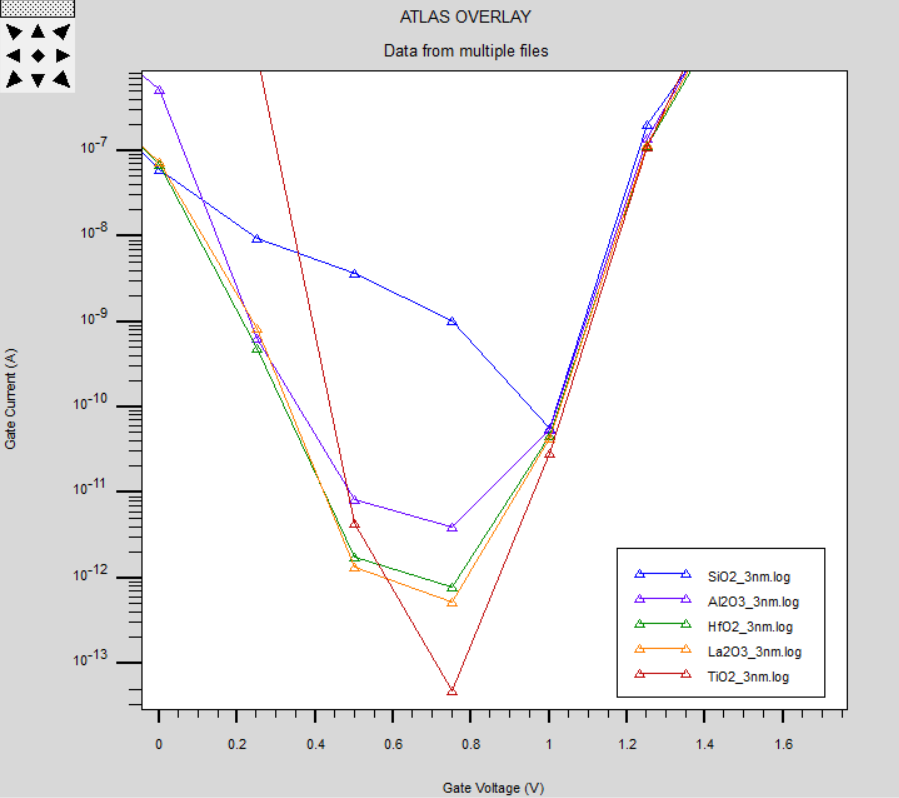
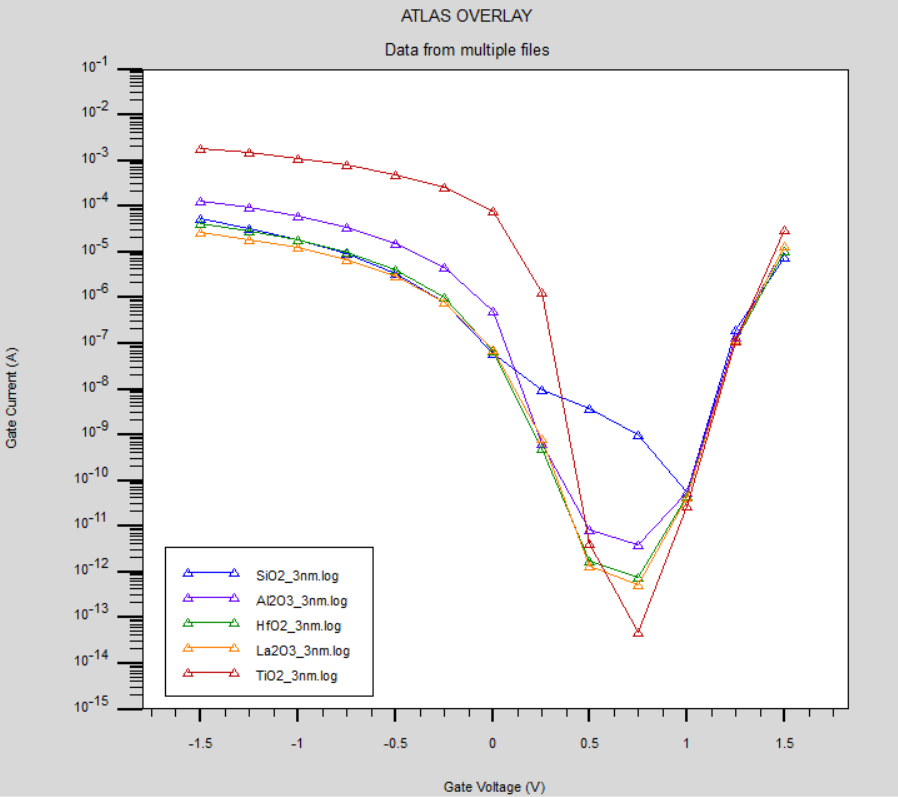
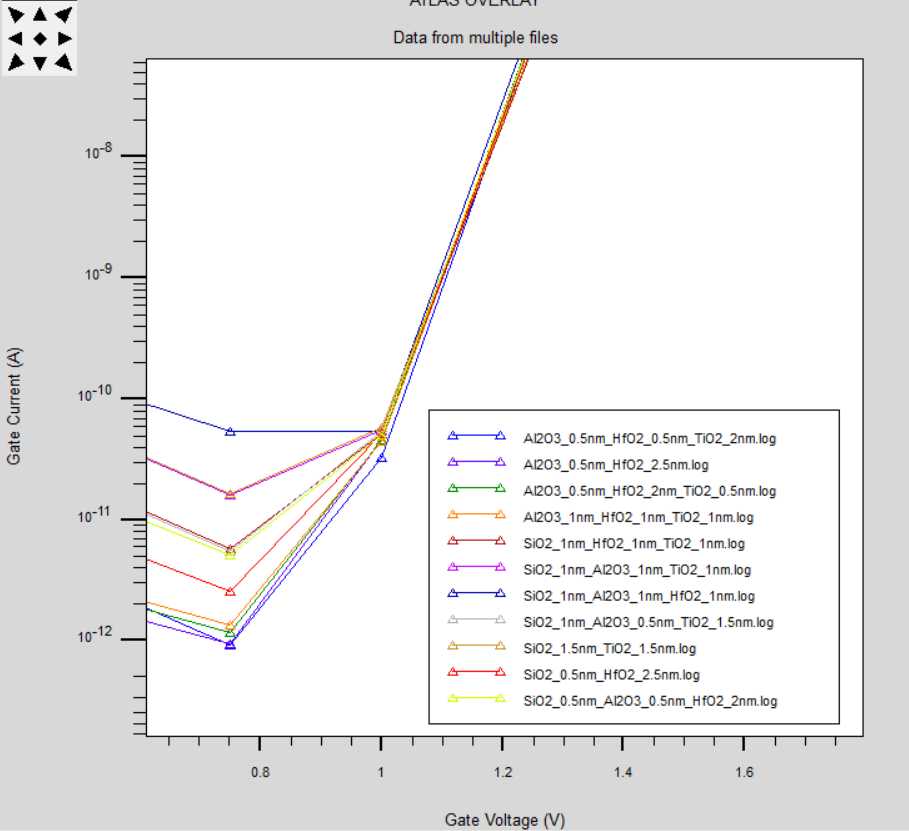
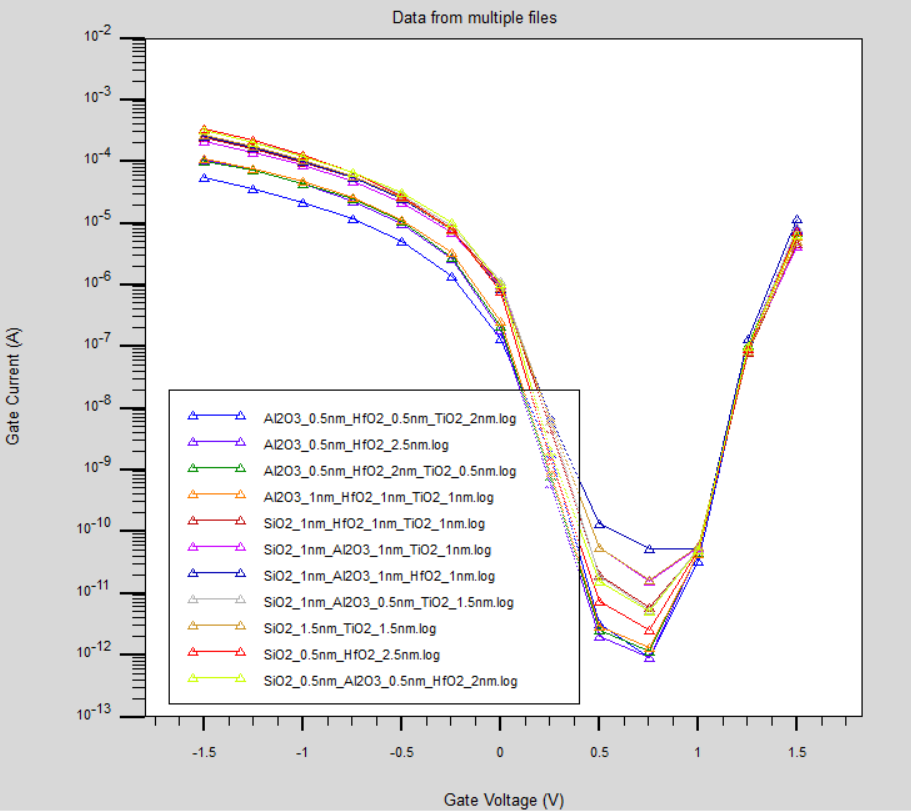
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Figure 6a. ID for single material gate oxide dielectrics (control group) log(ID) –VGS (left) and ID –VGS (right)

b. ID current for FGM-group of gate oxide dielectrics log(ID) –VGS (left) and ID –VGS (right)



1. (b)



(c) (d)

Figure 7a, 7b (zoom): IG leakage current for single material gate oxide dielectrics (control group) log (IG) –VGS

7c, 7d (zoom): IG leakage current for FGM group gate oxide dielectrics, log (IG) –VGS

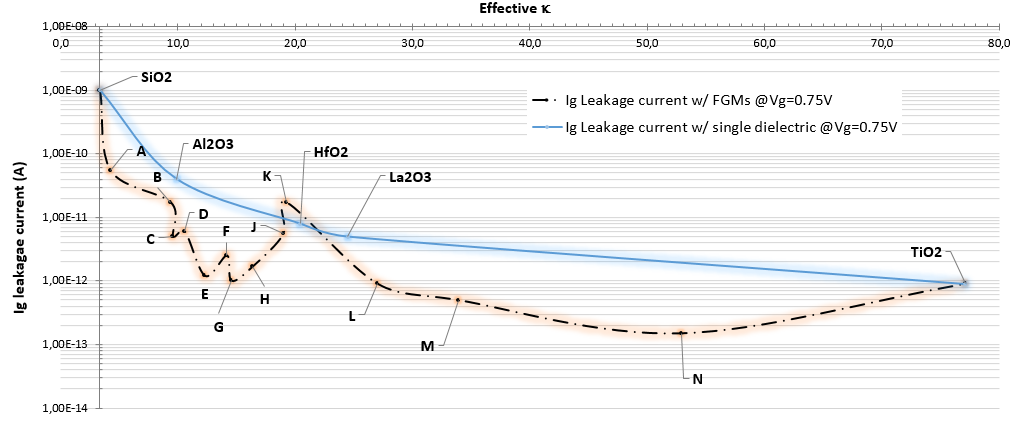


Figure 8. Ig Leakage Current for FinFET with single material and FGM gate oxide dielectrics

(calculated with MG model)

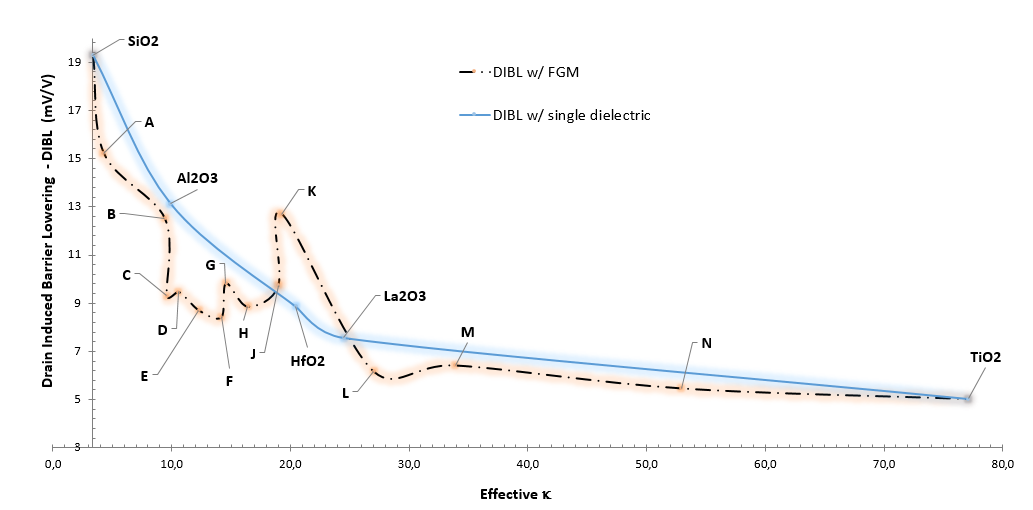
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Figure 9. DIBL with single material and FGM gate oxide dielectrics (calculated with MG model)

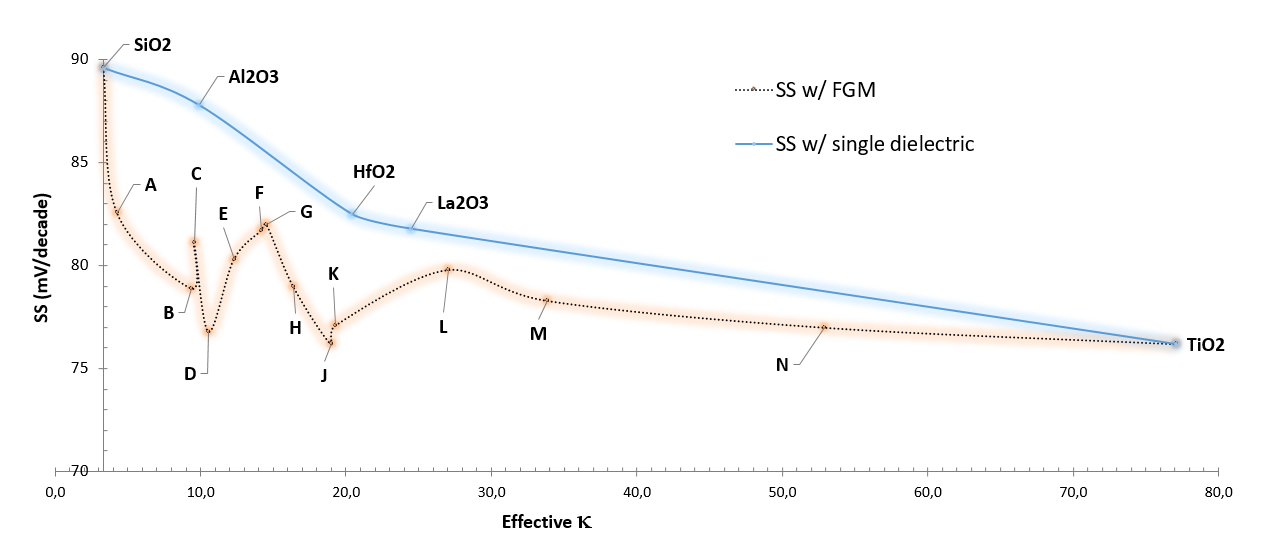
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Figure 10. SS with single material and FGM gate oxide dielectrics (Effective calculated with MG model)

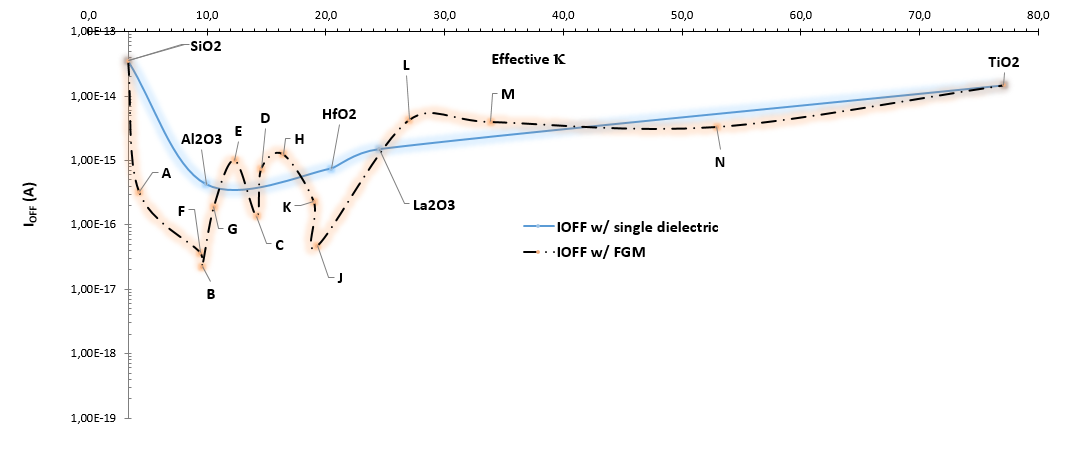
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Figure 11. IOFF with single material and FGM gate oxide dielectrics (Effective calculated with MG model)

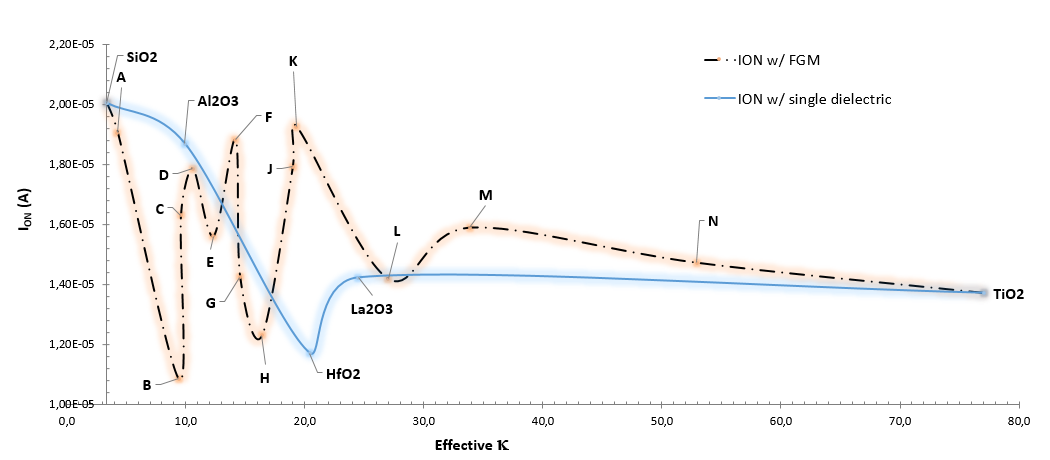
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Figure 12. ION with single material and FGM gate oxide dielectrics (Effective calculated with MG model)

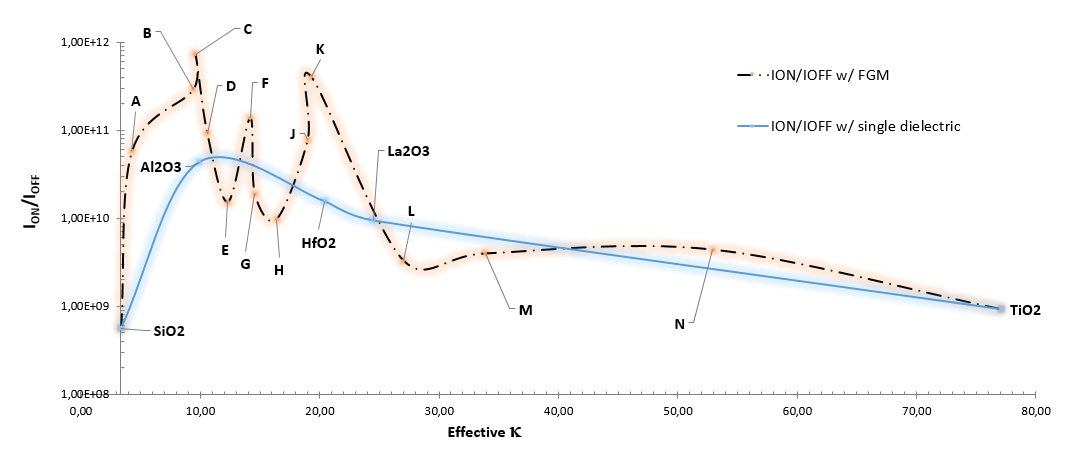


Figure 13. ION/IOFF ratio with single material and FGM gate oxide dielectrics (Effective calculated with MG model)

1. **Threshold Voltage VTH**

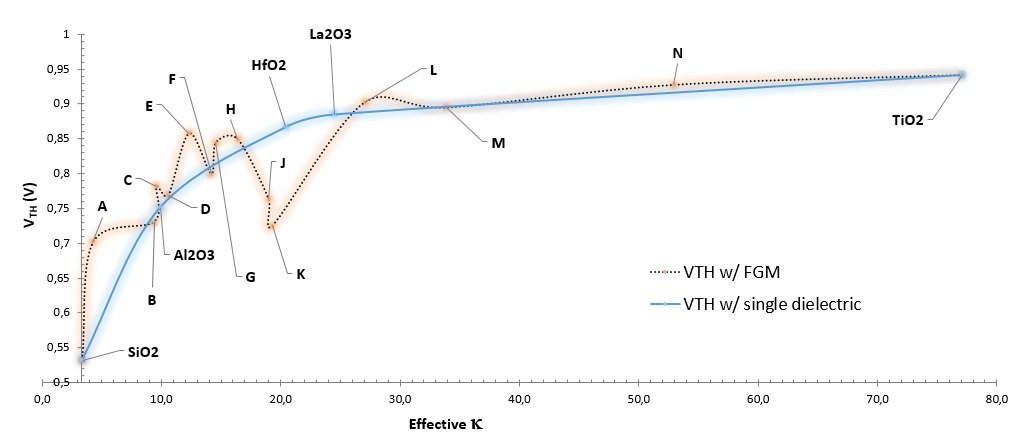


Figure 14. VTH with single material and FGM gate oxide dielectrics

Table 5. values for each configuration of single dielectric and FGM configurations.

|  |  |
| --- | --- |
| **Material** | **FOM\_FET** |
| **SiO2** | **9,5** |
| **Al2O3** | **20,6** |
| **HfO2** | **33,4** |
| **La2O3** | **43,0** |
| **TiO2** | **76,0** |
| **FGM-A** | **20,0** |
| **FGM-B** | **70,2** |
| **FGM-C** | **70,9** |
| **FGM-D** | **38,4** |
| **FGM-E** | **45,6** |
| **FGM-F** | **38,0** |
| **FGM-G** | **58,0** |
| **FGM-H** | **41,6** |
| **FGM-J** | **40,3** |
| **FGM-K** | **56,1** |
| **FGM-L** | **65,9** |
| **FGM-M** | **69,3** |
| **FGM-N** | **100,0** |